NASA Contractor Report 195338

Power and Spectral Efficient Advanced High Data Rate Modem

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Microwave Monolithics, Inc.
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June 1994

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Prepared for
Lewis Research Center
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1) INTRODUCTION

The exponentially increasing demand to transfer massive amounts of data between world wide destinations generated by sophisticated space and ground based high resolution multi-band sensors, interactive multi-media, computer network interlinks, and wireless trunkline systems is severely straining the available microwave bandwidth, which can only grow linearly by costly extension into the millimeter-wave bands. Power and spectrally efficient, high data rate modems are thus essential, particularly at high concentration "bottle necks" which typically occur in the space segment of communications backbones such as those planned for deployment over the next decade.

A number of spectral modulation techniques have been previously used to reduce the modulation bandwidth of digital data links. The most notable are based on MPSK and QAM modulation techniques. However with these approaches, extensive filtering must be performed on the modulated signal to achieve a bandwidth efficiency of 2 bits per hertz. This filtering causes inter-symbol interference (ISI) to be introduced into the waveform, and introduces AM on the signal constellation. For ideal systems the ISI can be compensated at the demodulator by using a complex matched filter. This, however, places a severe burden on the receiver filters, which must simultaneously act as matched noise filters. Power hungry, linear (Class A) amplifiers are often required for such systems.

Prior to program phase I, Microwave Monolithics Incorporated (MMInc.) identified an attractive approach to the implementation of practical, bandwidth efficient, high data rate modems. The potential advantages of this approach become readily apparent by considering theoretical bandwidth efficiency and noise performance for the various techniques. The theoretical unfiltered spectral efficiencies are: 1/2 bit/Hz for BPSK, 1 bit/Hz for QPSK, 1.5 bits/Hz for 8PSK, and 2 bits/Hz for MMInc.'s approach. Furthermore, and 8PSK system is about a dB worse (related to Eb/No) than MMInc.'s approach at a bit error rate of 10^{-6}. Thus, the QPRS modem is inherently more bandwidth efficient and less sensitive to noise than the more traditional 8PSK modem. More

complex signal constellations, such as 16PSK, could not provide the necessary noise immunity, even with extremely complex filtering schemes.

Preliminary computer analysis of the MMInc.'s approach further supported the concept, therefore MMInc. fabricated a low frequency, low data rate, bandwidth efficient breadboard modem to experimentally examine its capabilities for satellite communications applications. Preliminary measured data was very encouraging, and the Phase I program reported herein was initiated to further demonstrate feasibility of the modem via continued computer simulations, more extensive characterization of the breadboard modem, and iteration of MMInc.'s high speed design of this modem.

The exciting results from program phase I have clearly indicated that a rugged, low power, bandwidth efficient, high data rate modem based MMInc.'s approach is ideally suited to advanced satellite communications systems, where bandwidth and prime power are at a premium. A phase II proposal has therefore been submitted to fabricate an engineering prototype of the high data rate bandwidth efficient modem designed in phase I, and deliver it to NASA.

Key performance goals for the bandwidth efficient, high data rate modem are summarized in Table 1-1. These goals, particularly bandwidth, IF frequency, and data rates, have been selected for maximum compatibility with on-going NASA programs, and to demonstrate the capabilities of the modem.

Table 1-1) Selected Technical Performance Goals

Preamble Length (Carrier and clock synchronization)	1000 symbols max.
Data Rate	800 Mbps \
Bandwidth	450 MHz /Case 1
Data Rate	400 Mbps \
Bandwidth	225 MHz /Case 2
Out of Band Power	-60 dBc max.
Implementation loss	< 3 dB from QPSK @ BER of 10^{-6} with AGWN
IF Frequency	3.239 GHz

2) SUMMARY

The objective of this SBIR phase I program was to demonstrate feasibility of the high data rate, bandwidth efficient modem via measurement of an existing low frequency breadboard modem and extensive computer simulations, and to use the experimental and CAD results to revise MMInc.'s high data rate modem design as necessary to prepare for fabrication in phase II. The statement of work which guided this effort is presented as table 2-1. Despite a severe interruption caused by the "Northridge" earthquake on January 17, 1994, all of these tasks have been completed, thus providing a strong foundation for the phase II program.

Discussions with NASA technical personnel have indicated that the originally proposed performance goals are appropriate for the engineering prototype hardware to be fabricated in phase II. Furthermore, measurements and computer simulations continue to indicate that these are realistic goals. Therefore as previously indicated in Table 1-1, no performance goal modifications have been made since submission of the phase I proposal.

MMInc.'s existing low frequency, low data rate modem has been extensively characterized, including experimental demonstration of the crucial carrier recovery loop based on a re-modulation, demodulation technique for phase locking of the reconstructed carrier. Performance of this loop tracks computer predicted performance well, as do the optimal settings of key gain and threshold values in both the modulator and demodulator. Validity of MMInc.'s computer models, both the custom modem simulator and the MATHCAD simulations, have thus been experimentally verified.

With enhanced confidence in the computer models, the program continued with computer simulation of various sub-optimum operating conditions to determine trade-offs between the various operating and design parameters. Preliminary values for all key bandwidth and threshold settings have been determined and incorporated into the high

speed modem design.

Two key facts emerged as these measurements and computer simulations continued. First, an enhanced data detection circuit is highly desirable. Although the originally proposed data detector is relatively simple and functions well under ideal conditions, a more robust design is needed for compatibility with realistic hardware implementations and operating conditions. A new data detection circuit has therefore been designed and incorporated into the high data rate modem design.

Second, although computer simulations are accurate and allow easy modification and control of all systems parameters (even modem architecture), they are extremely time consuming. This is particularly true for bit error rate calculations, which can take weeks of computer time on modern workstations. The need for a low frequency modem which can be modified with moderate difficulty, such as MMInc.'s breadboard, has thus become even more apparent. Although not originally proposed as part of the phase I effort, MMInc. decided to construct a second generation low data rate, bandwidth efficient modem which is more versatile than the original. Fabrication of this second generation breadboard modem, which operates at a somewhat higher carrier frequency and data rate to ease experimentation, is already well under way, thus providing a "head start" for program phase II.

Table 2-1) Phase I Statement of Work

Task 1) Assess NASA and commercial performance requirements for the low power spectrum efficient high data rate modem, and, in consultation with NASA technical personnel, finalize the modem performance goals.

Task 2) Complete characterization of the existing low data rate bandwidth efficient breadboard modem for performance in the presence of channel noise. Utilize this breadboard to experimentally derive key operating parameters and/or support computer simulation results.

Task 3) Utilize computer simulations to estimate sensitivity to critical fabrication tolerances for the low power and spectrum efficient high data rate modem, and identify optimal set points for the operating parameters.

Task 4) Utilizing design and implementation techniques to minimize prime power consumption, refine MMInc.'s preliminary high data rate modem design and estimate performance characteristics.

Task 5) Deliverables:

A) A final report will be submitted within 30 days of completion of the technical effort.

3) Theory of Operation

To circumvent the difficulties associated with more traditional high data rate modem designs, particularly spectral efficiency and noise susceptibility, MMInc.'s approach is based on low power Quadrature Partial Response Signaling (QPRS), which is inherently superior in both of these the critical areas. Without filtering, this approach provides a theoretical performance (related to Eb/No) just 2.4 dB worse than QPSK, and has a bandwidth efficiency of better than 2 bits/Hz. Theoretical bit error rate performance of this modulation scheme in the presence of AGWN (noise) is summarized in Figure 3-1. For comparison, the theoretical performance of QPSK and 8PSK systems are include in this figure.

Partial Response Signaling was proposed by Lender in the early 60's [1]. It was shown that a signal of 2*BW symbols per Hz could be transmitted in a bandwidth of BW hertz with no inter-symbol interference (ISI) without using infinitely sharp filters. This technique was called duobinary signaling or correlative coding. The basic process behind the technique is to introduce a controlled amount of ISI into the signal spectrum. By introducing correlated interference between pulses, and by changing the detection process, it is possible to achieve an ideal symbol rate of two symbols per hertz without band limit filtering. Since the bandwidth efficiency is inherent in the approach, filter design is considerably simplified compared to the case of the more traditional 8PSK modulation scheme.

The process of duobinary coding will now be described in detail. A partial response system generates an L-level signal from a binary bi-level data source (+/-1) using a linear weighted superposition of the input symbols Xi, where the superposition memory extends over an n bit period, ie:

$$Yi = K1*X1 + K2*Xi-1.....+Kj*Xi-j+1$$

The duobinary transfer function can thus be described as a digital filter incorporating an (n) bit delay, followed by a an ideal rectangular transfer function. For the modem MMInc. has designed and analyzed in program phase I, n=1. The Fourier transform of a one bit delay is:

$$e^{-j2\pi fT},$$

thus the duobinary transfer function is:

$$H1(f) = 1 + e^{-j2\pi fT}$$

Since the transfer function of an ideal rectangular filter H2(f) is:

$$H2(f) = T \quad \text{for } |f| < 1/2T, \quad 0 \quad \text{elsewhere,}$$

the overall transmit transfer function, which consists of the composite of H1(f) and H2(f), can be expressed as He(f) = H1(f) * H2(f), or (after some algebra):

$$|He(f)| = 2T \cos(\pi fT) \text{ for } |f| < 1/2T, \quad 0 \text{ elsewhere}$$

From this function, it is clear that quadrature modulation will lead to a bandwidth efficiency of 2 bit/Hz. Hardware and computer models of this modem, including measured and simulated spectrums clearly demonstrating the 2 bit/Hz bandwidth efficiency, are presented in subsequent sections of this report.

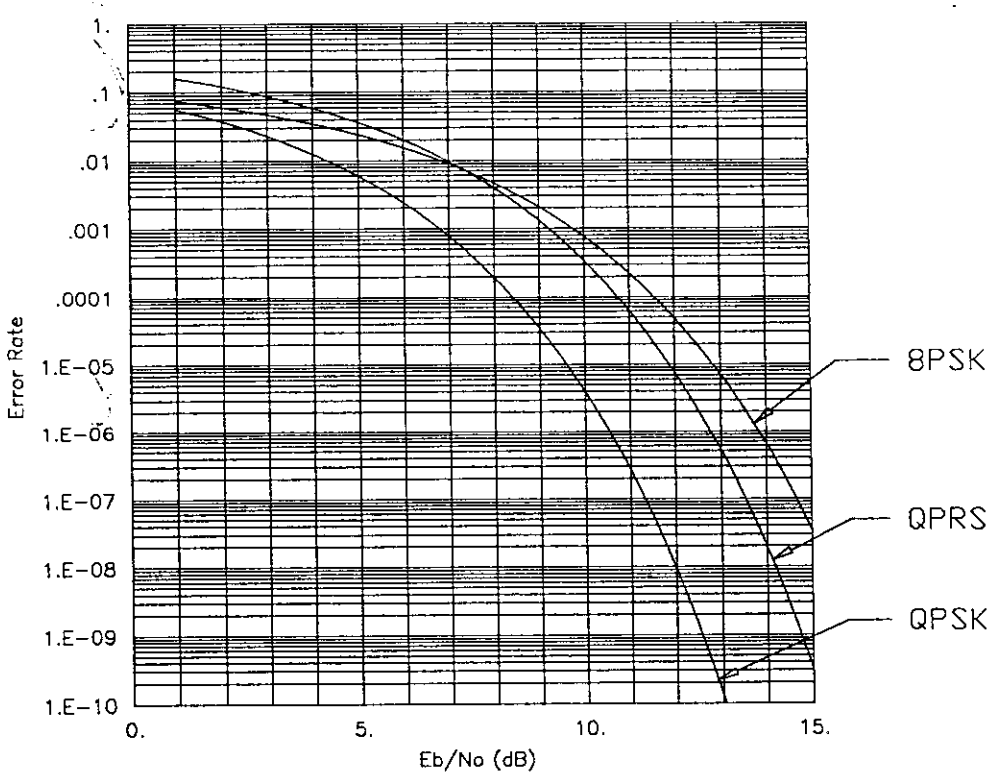

Figure 3-1) Comparison of Theoretical Performance Characteristics of BPSK, QPSK, 8PSK, QPRS in the Presence of Noise.

4) High Data Rate Bandwidth Efficient Modem Design

The QPRS modem design presented in the phase I proposal has remained essentially unchanged, however operating parameters and circuit details have been refined throughout this program. In addition, an enhanced data detection circuit has been adopted for improved performance in the presence of noise.

The modem design is summarized in this section, starting with the modulator in section 4.1, followed by the demodulator in section 4.2.

4.1) QPRS Modulator

The QPRS modulator encodes the 800 Mbps data stream into two duobinary coded channels. These channels, after filtering, drive the I and Q inputs of the quadrature modulator. The combined signal then passes through a cleanup filter, and becomes the modem output. The modulator thus consists of three parts; input logic, QPRS coder/modulator, and the control and status module. A schematic of this modulator design is shown in Figure 4.1-1.

The input logic is designed to keep data edges bit synchronous by re-clocking all data brought into the module. Separate clock drivers are used for this purpose. An input multiplexer allows for a forward error correction module to be switched in for error encoding. The module also includes differential signal precoding. Clocks are provided by the data sources.

The QPR encoder module duobinary encodes, filters, and modulates the data. The clock is buffered and synchronously reclocks the data into the coder. The output of the registers of the coder are bilevel coded using, for example, an ECL current switch quantizer. The output of these quantizers are summed to form the tri-level (D+1) code: +2,0,-2. The output signal from the coder is then filtered by a lowpass filter with a bandwidth of 1/2T. For PRS signaling the filter does not

cause undo phase distortion at the band edge due to the inherent roll off of the duobinary coded waveform. The filtered I/Q channels modulate the quadrature modulator to form the QPRS signal S(t). As with QPSK and 8PSK systems, phase balance of the modulator is critical to proper operation (less than 2 degrees of offset).

The modem rate switching is accomplished by changing clock rates and by switch selecting the filters in the partial response coder. Note that for partial response the second transmit filter is not critical, and it is possible to change data rates without affecting performance as long as the range is not greater than 2:1. This feature would allow for switching in a convolutional coder of rate 3/4, 7/8 without changing the precoder filter.

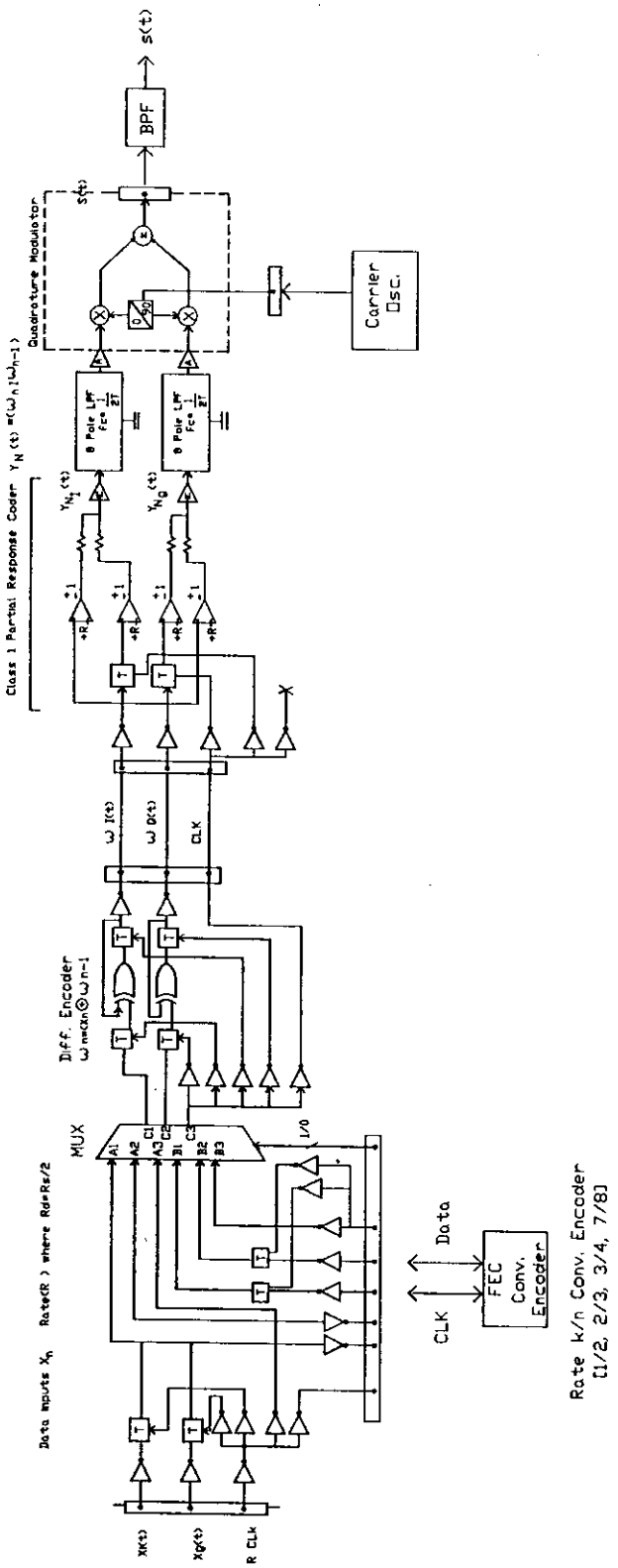

Figure 4.1-1) QPRS Modulator Design

4.2) QPRS Demodulator

The demodulator is designed as a complete unit including input I/F with coherent AGC, QPRS demodulation, a carrier recovery loop, bit synchronizer, and data detection module. A block diagram is shown in Figure 4.2-1.

The IF module has an input of 3.239 Ghz, with a bandpass noise reduction filter to reduce the input noise bandwidth to just under 2/3T. An AGC amplifier follows the filter. The coherent AGC amplifier derives it's feedback control signal from the detected data. The AGC is a critical part of the detection process for the modem, especially when forward error correction is used. It provides a method of adaptive threshold detection by keeping the envelope of the demodulated data at a fixed level independent of the input signal, within the 30 dB dynamic range of the amplifiers.

The carrier recovery loop is the most critical portion of the QPRS modem. Estimates of performance degradation due to carrier offset have been made by Taylor and Cheung[2], and they show the importance of good carrier recovery. A phase errors of 6 degrees can cause performance degradation of a dB or more at an error rate of 10^{-6}. A data aided remodulator, shown in Figure 4.2-2, is used for the carrier recovery loop. The basic principal of the loop is to remodulate the received signal R(t) with an estimate of the recovered data. This loop uses a three level limiter to estimate the remodulation signal. The quantized signal modulates a delayed R(t), the remodulated I/Q signal is quadrature summed, and a collapsed estimate of the carrier is filtered and phase-locked to form the coherent carrier reference. The critical part of this loop is maintaining phase balance in the quadrature demod and remodulator circuits. A phase balance of less than 3 degrees is desired. An advantage of this loop is that all multipliers are A/C coupled, hence balanced mixers can be used. A second advantage is that a loop lock detector signal can be implemented by taking a quadrature estimate of the collapsed carrier and the phase-locked carrier reference. Proper performance of this loop has been demonstrated by CAD

techniques, and has also been demonstrated experimentally with MMInc.'s breadboard QPRS modem. This is discussed in more detail in subsequent sections.

The phase demodulator is identical to the phase modulator used in the modulator, and must be built with careful attention to phase balance between the 0 degree and 90 degree splitters. A noise filter is used to band limit the channel noise. The noise samples will be independent since the noise has been band limited to the Nyquist frequency (pi)/T, and the transmitter filter and the channel determine the shape of the frequency response.

The level quantizer switches about the levels +/-r volts, and forms a Tri-level signal of +1,0,-1. Multiplying both I/Q quantized signals by R(T) and quadrature summing results in a reconstructed carrier reference of the form: $(|A(t)|+|B(t)|)\sin(Wt+dW+P)$. This signal is then filtered using a phase locked loop, and the filtered reference is feed back to the quadrature demodulator. The three level quantizer is an important feature of the demodulator. This current mode switching circuit must have switching times on the order of 200 pico seconds, thus FETs are employed as current switches followed by comparator amplifiers. With both current switches off, a bias current flows through the load resistor resulting in a +v reference voltage. As either or both switches are turned on a zero or minus voltage is generated, thus forming the three level signal. The differential comparator consists of a pair of cascoded differential current mode amplifiers.

The data bit synchronizer, shown in Figure 4.2-3, is designed using a transition detection loop. This loop is basically a data transition detector followed by a phase locked loop filter. The differentiator senses data transitions and rings up the transitions using a high Q bandpass filter at I/2Ft. This signal is then phase locked to the clock reference. The PLL acts as an additional high Q filter. This circuit works well even in high signal to noise ratio (>10 dB) situations.

An estimate of bit clock lock is derived by taking a quadrature estimate of the incoming data transition signal. This estimate has a maximum value at phase lock, hence the signal can be lowpass filtered and detected.

The data detector, shown in Figure 4.2-4, follows the data matched filter. The filter is optimized to noise filter the recovered data symbol as well as equalize the recovered data pulse if required. For pre-coded Class one partial response the bit decoding can be simple, although, as described later, somewhat more complex schemes will prove advantageous. In its most simple form, the data decision is based on:

$$\text{if}(-r < X'(t) < +r), \text{ then "1", else "0"}$$

where +/-r is a reference voltage equal to a derived threshold.

The AGC feed back to control the demodulator input signal level is critical for proper operation of the modem. A simple method of providing this is to use a received data estimate of both I and Q. From the soft decision of the data detector, we get an estimate of the |I| and |Q| least three (3) significant bits. The coherent data signal derived AGC control is taken from the sum of |I|+|Q|. In the breadboard modem, a simplified version of this circuit based on a non-linear "absolute value" circuit has been implemented, and even this approach appears to work well.

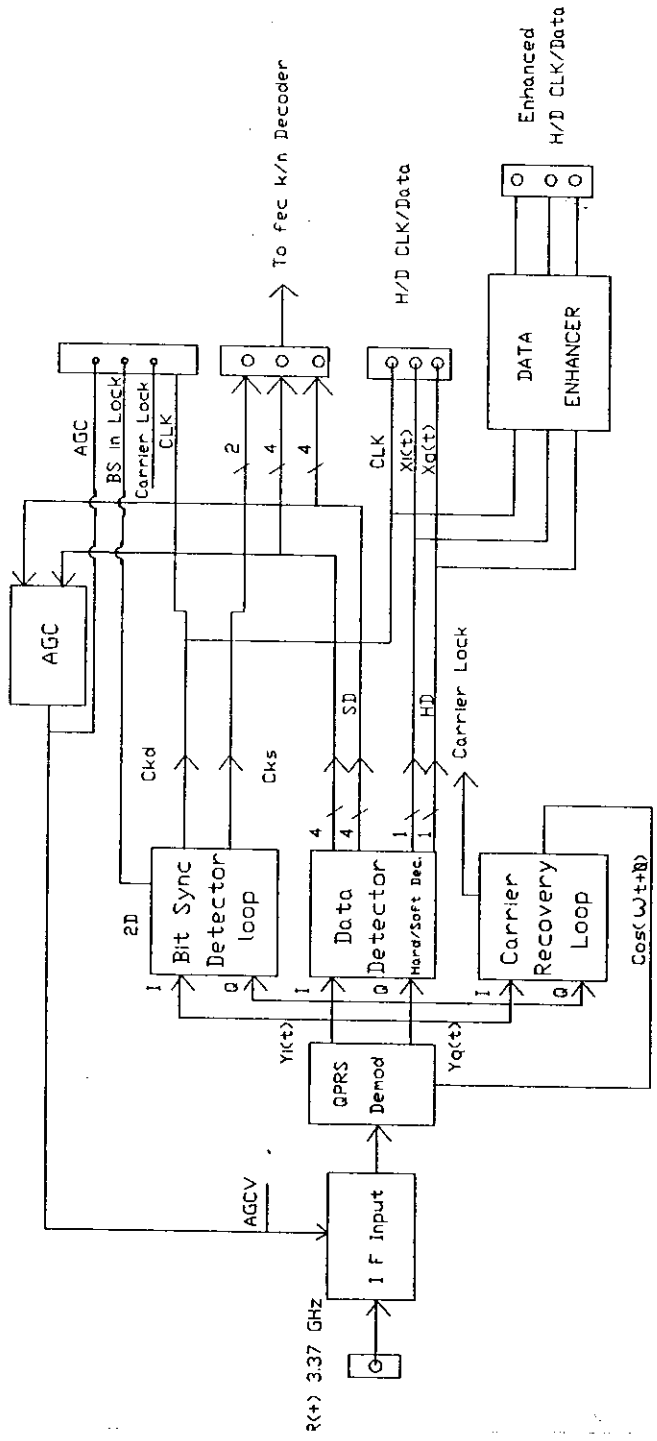

Figure 4.2-1) Block Diagram of the QPRS Demodulator.

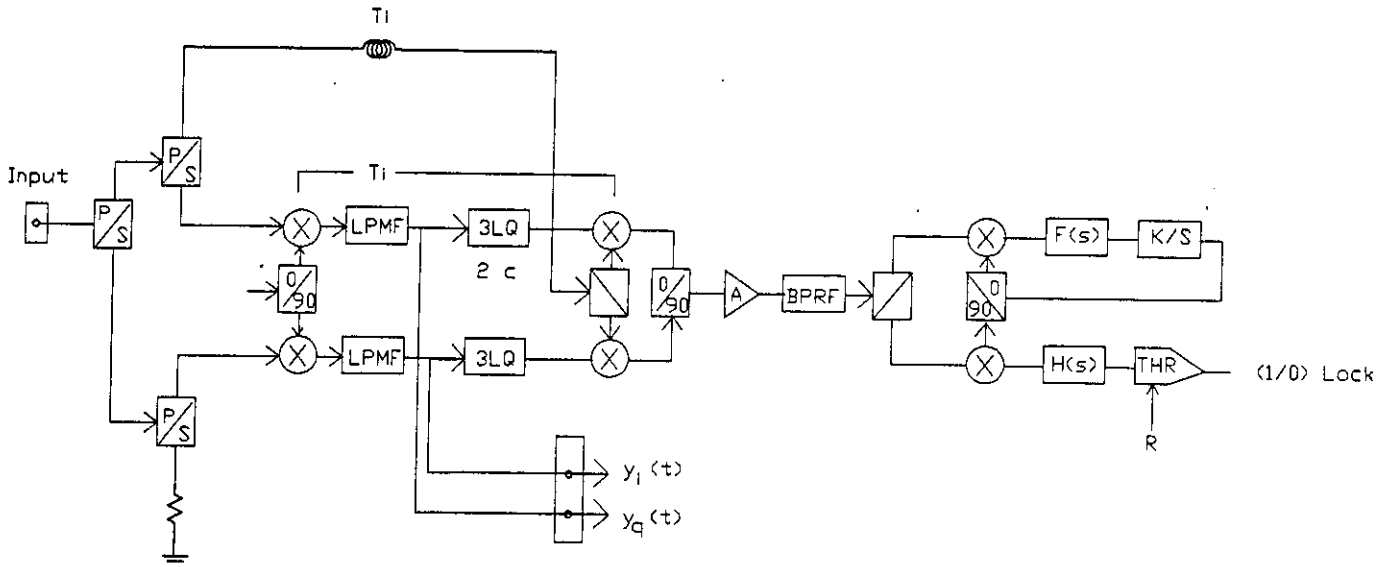

Figure 4.2-2) Data Aided Remodulator - Demodulator Loop

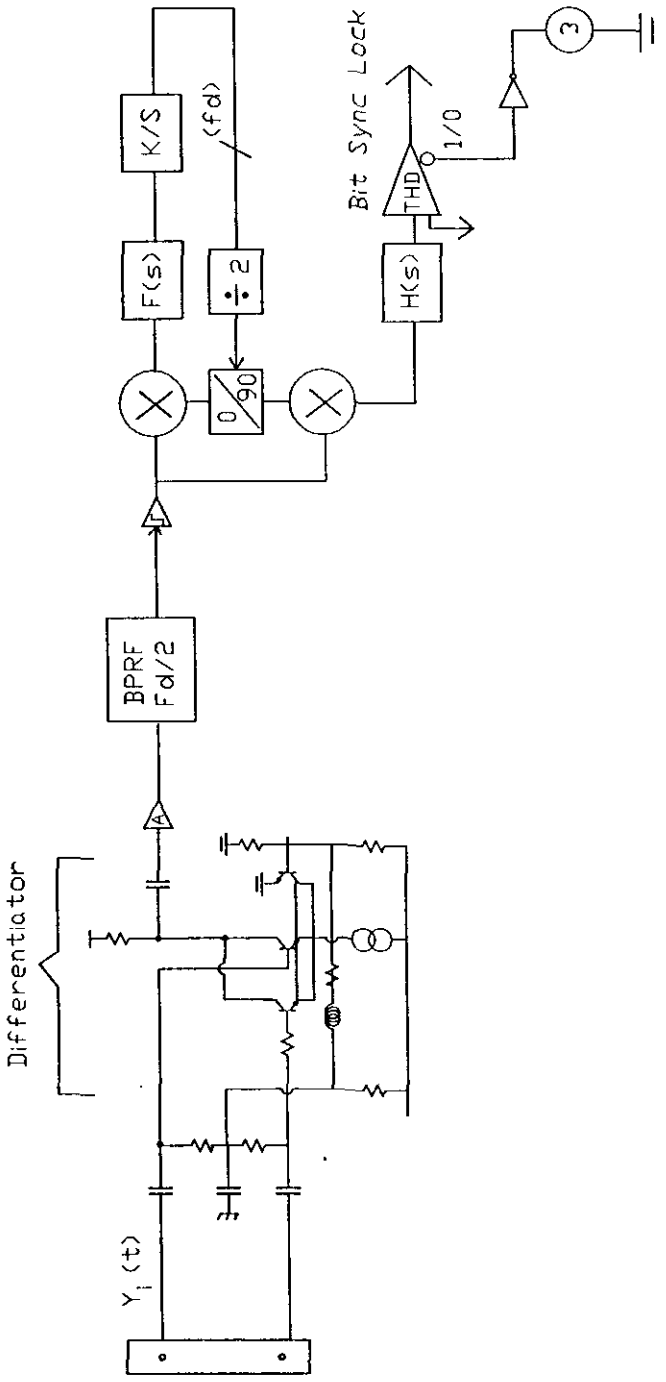

Figure 4.2-3) Bit Synchronizer Loop

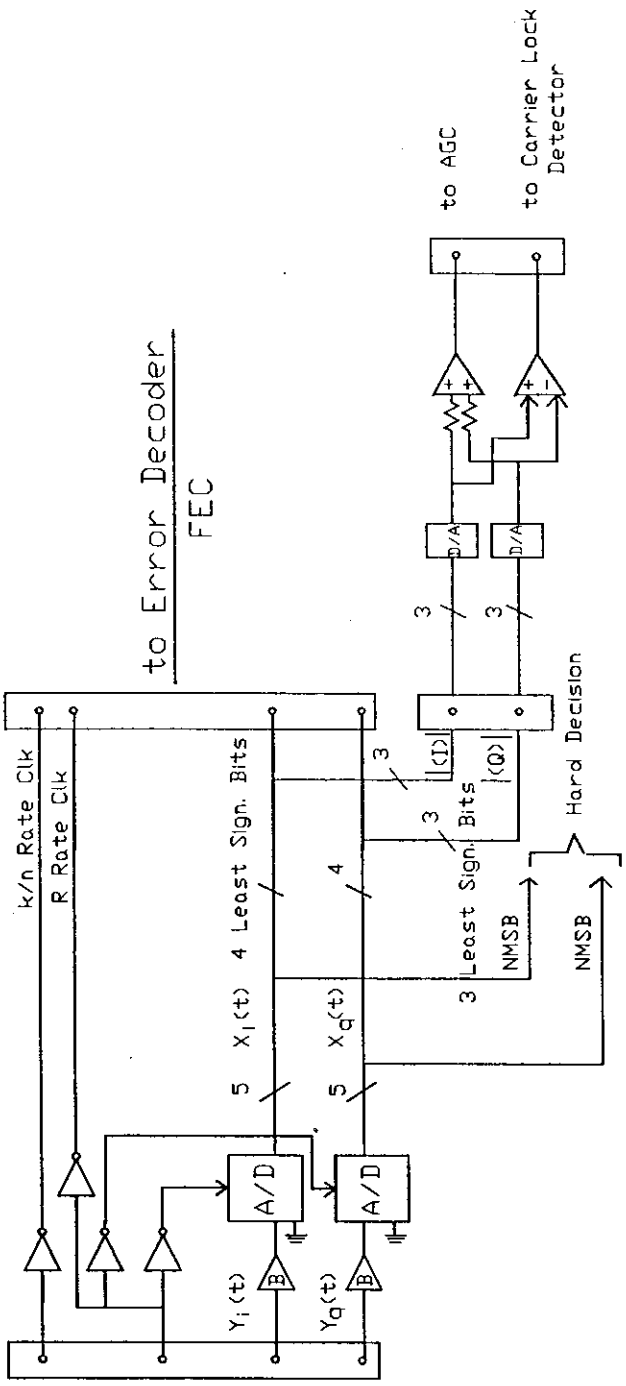

Figure 4.2-4) Block Diagram of the Data Detector

5) Measurements of Low Data Rate Bandwidth Efficient Breadboard Modem

MMInc. has evaluated performance of the breadboard modem at all key points along the data path of both the modulator and demodulator. As described later, these measured results are in excellent agreement with computer simulations. All measurements presented in this section were taken with the remodulator/demodulator carrier recovery loop in operation, clearly indicating that this crucial loop operates as predicted by the MATHCAD simulations presented later.

To demonstrate operation of the QPRS modem, and provide a clearer picture of the underlying operating principles involved, Figure 5-1 through Figure 5-10 present a sequence of measured signal waveforms at selected points in the data path.

Figure 5-1 is a photograph taken from an oscilloscope, showing the modulators differentially encoded input data stream for the "I" channel in the bottom half of the photo and the QPRS (D+1) tri-level signal generated from this data stream in the top half of the photo. The amplitude-phase constellation of these I/Q transmit signals is shown in Figure 5-2. Note the anticipated nine point pattern, and the near perfect symmetry which is achieved when the drive signals are properly adjusted for amplitude and offset.

As previously described, these I and Q signals modulate the IF carrier (10 MHz for this breadboard modem) via an I/Q modulator. The IF signal then passes through a channel simulator which provides attenuation and the ability to add white noise. A photograph of the resulting modulator output spectrum (prior to filtering of any kind) as measured on a spectrum analyzer without additive noise is shown in Figure 5-3. As shown in this figure, the unfiltered spectrum has its first nulls at $\pm$35 KHz around the carrier frequency, for a total bandwidth of 70 KHz. Since the bit rate for each of the I and Q signal channels was set at 70 KHz for this measurement, the modems bandwidth efficiency of 2 bits/Hz is evident. Also note the imbalance in the

output spectrum caused by slight amplitude and phase imbalances in the I/Q modulator. Obtaining and/or fabricating highly balanced I/Q mixers is one of the key requirements for successful high data rate QPRS modem implementation in program phase II. Figure 5-4 shows a spectrum of the same signal, but with additive white noise, sampled at the output of the demodulators AGC amplifier. At this measurement point the combined signal plus noise has been partially band filtered by the pre-filter of the AGC circuitry, but the increased noise floor is clearly visible.

After passing through an AGC amplifier to set the received signal to a fixed level, the demodulator mixes a reconstructed carrier with the incoming signal in an I/Q demodulator. The demodulated I and Q baseband signals are low pass filtered, and representative eye diagrams are shown in Figure 5-5, with the I and Q channels on the top and bottom. For reference, the data clock signal is shown in the center of this photograph. A similar photograph, taken after the introduction of white noise, is shown as Figure 5-6.

A photograph of the amplitude-phase constellation of the received I and Q baseband channels is show in Figure 5-7. As for the modulator, slight amplitude, phase, and offset errors, which are accumulated from both the modulator and demodulator, are evident in this photograph. A photograph of the same constellation, after the introduction of white noise in the channel, is shown in Figure 5-8.

To clarify how the data decoding circuitry operates, the received I channel signal is shown at the top of the photo in Figure 5-9, the clock signal is shown in the center, and the corresponding decoded data is shown at the bottom. Note that the characteristics of the waveform at the top of the photo are similar to the (D+1) waveform originating in the modulator, although the exact shape is different since this sample is from a different portion of the originating pseudo-random data stream. As shown at the bottom of this photo, a digital "1" (high) is generated when the received signal is either above the positive threshold or below the negative threshold, and a digital "0" (low) is generated otherwise. Note also that the digital output signal shown at

the bottom of this photo is delayed by one clock cycle due to the reclocking circuitry in the data decoder logic.

A similar photo, taken at a different portion of the data stream, was taken after the introduction of white noise. This photo is shown in Figure 5-10. As expected, the I waveform becomes noisy, however the data is correctly decoded as shown at the bottom of the photo.

The demodulator in MMInc.'s breadboard modem does not contain a data clock recovery loop, therefore the above measurements were taken with the clock feed forward from the modulator. It was thus not possible to make bit error rate measurements since the phase of this low frequency clock could not be adjusted to the required value. Extremely long, adjustable, delay lines would be needed for this adjustment.

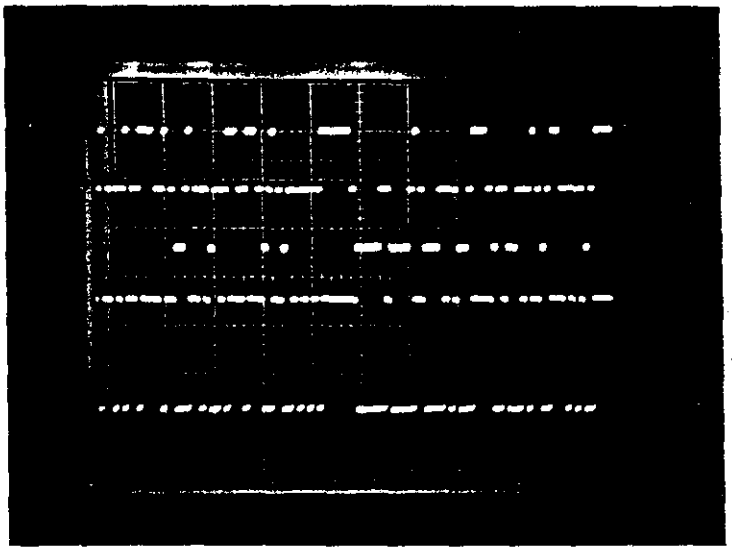

Figure 5-1) Photograph showing the breadboard QPRS modulators
TOP: I channel differentially encoded data stream
BOTTOM: (D+1) signal generated from this data stream

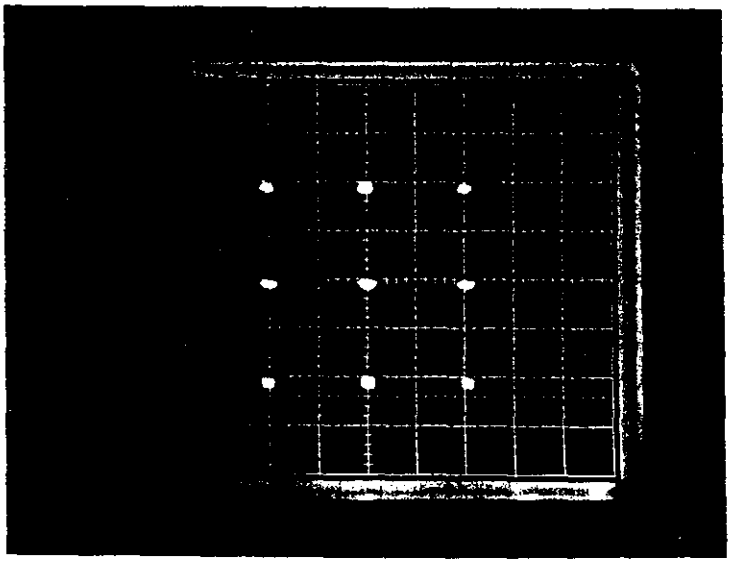

Figure 5-2) Photograph of the Breadboard QPRS Modulators
Amplitude-Phase Constellation

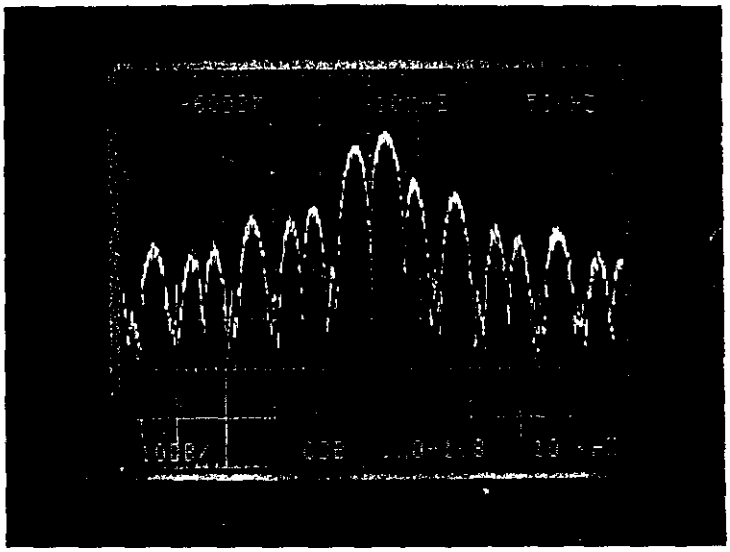

Figure 5-3) Measured Unfiltered Transmit Spectrum of the Breadboard QPRS Modulator without Additive Noise

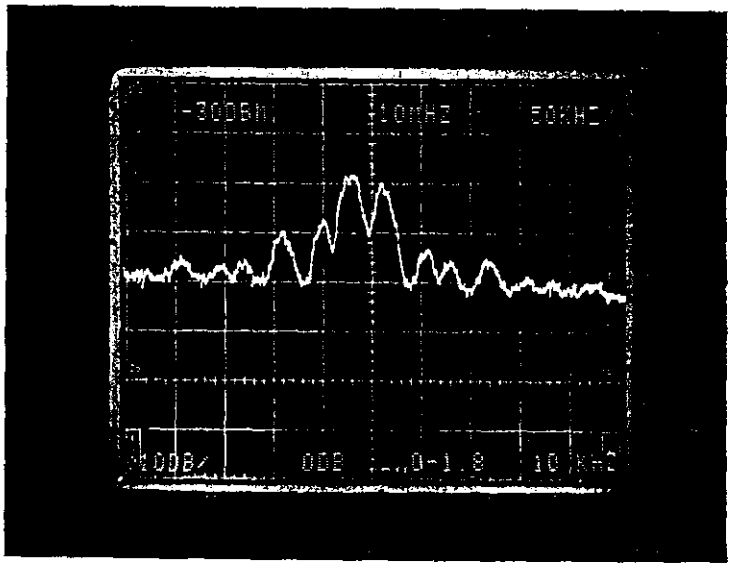

Figure 5-4) Measured Received Spectrum of the Breadboard QPRS Demodulator with Additive Noise and Pre-filtering

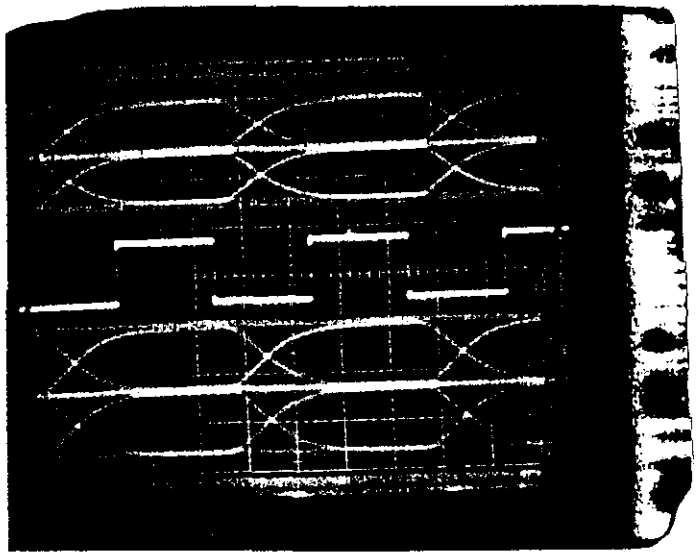

Figure 5-5) Photograph of Measured Breadboard Demodulator EYE Diagram without Additive Noise

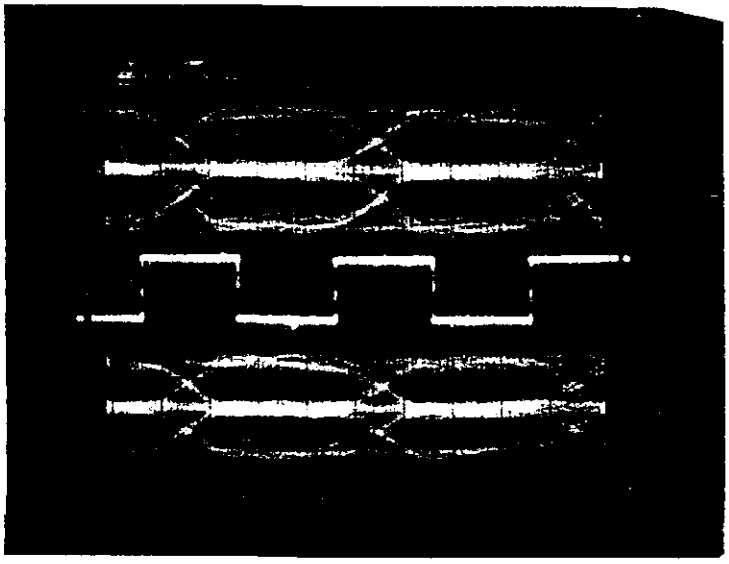

Figure 5-6) Photograph of Measured Breadboard Demodulator EYE Diagram with Additive Noise

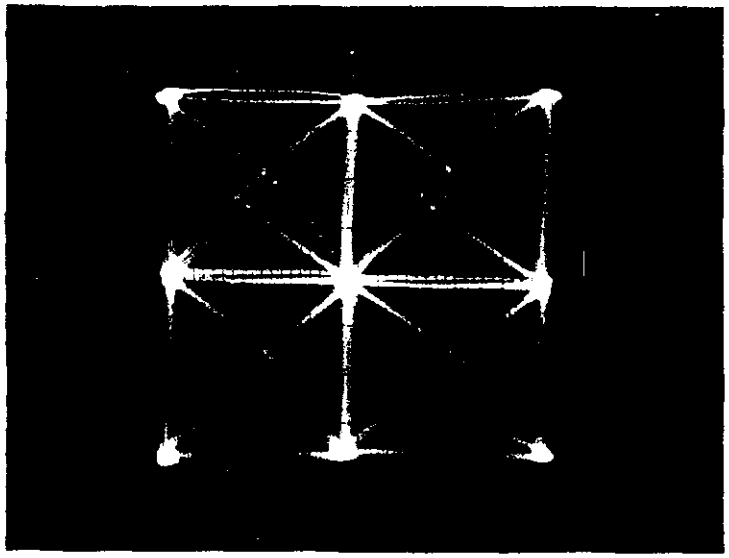

Figure 5-7) Photograph of the Breadboard QPRS Demodulators
Amplitude-Phase Constellation without Additive Noise

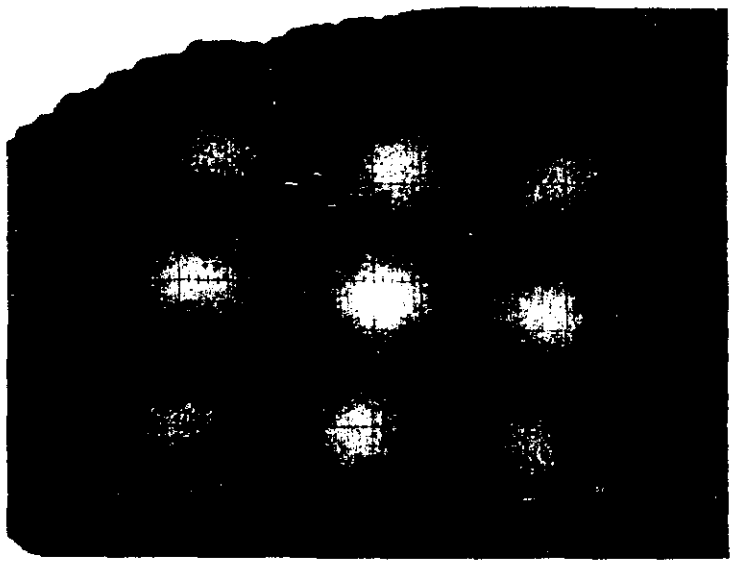

Figure 5-8) Photograph of the Breadboard QPRS Demodulators
Amplitude-Phase Constellation with Additive Noise

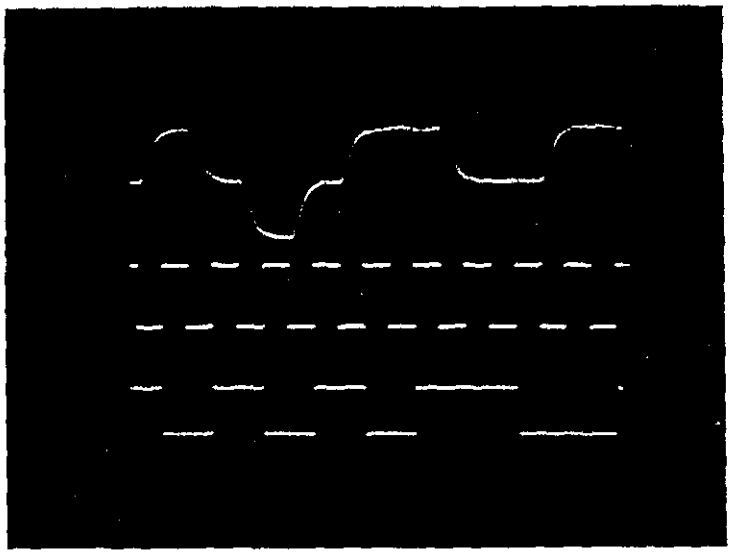

Figure 5-9) Measured Waveforms Depicting QPRS Data Decoding
Without Additive Noise
TOP: Demodulator I Channel Signal
CENTER: Data Clock
BOTTOM: Decoded Data Stream

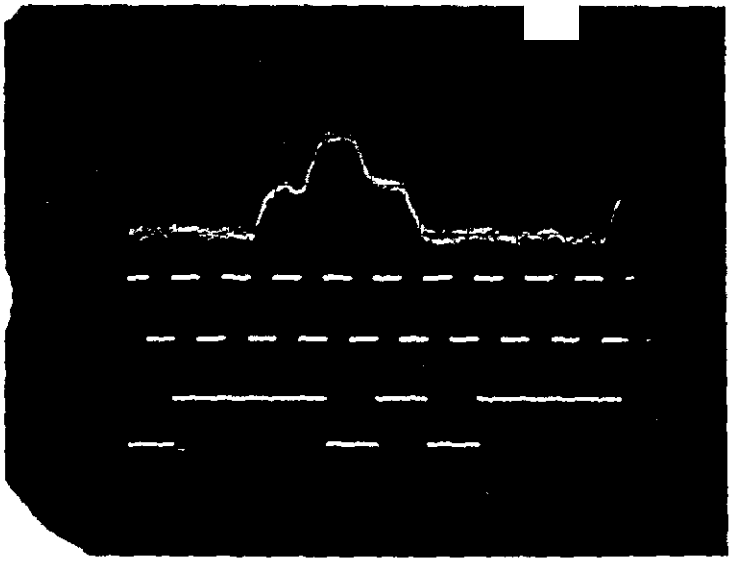

Figure 5-10) Measured Waveforms Depicting QPRS Data Decoding
With Additive Noise
TOP: Demodulator I Channel Signal
CENTER: Data Clock
BOTTOM: Decoded Data Stream

6) High Data Rate Modem Computer Simulations

Computer simulation of the QPRS modem were performed in two ways. The MATHCAD program was used to verify functionality of all key parts of the modem, including spectral efficiency, data path properties, and carrier regeneration. A custom modem simulator was then used to simulate the entire data path and perform bit error rate calculations under a variety of simulated operating conditions. These simulations are summarize in the following sections.

6.1) MATHCAD Functionality Verifications

A MATHCAD simulation of the QPRS modem has been developed. The main purpose of this simulation was to rapidly investigate alternative carrier recovery schemes, and select one for implementation in program phase II. Functionality of other key blocks of the modem was, however, also verified as a by-product of the simulation. This is demonstrated in a series of plots produced by the MATHCAD program.

In Figure 6.1-1, the modulators (D+1) simulated waveform is shown, followed by the modulators amplitude phase constellation in Figure 6.1-2. A plot of the simulated QPR modulated wave form is next shown in Figure 6.1-3, followed by a Fast Fourier Transform (FFT) of this waveform in Figure 6.1-4. Note that the spectral efficiency is 2 Bits/Hz as expected from the QPR signaling algorithm. Following demodulation, the received baseband tri-level waveform is shown in Figure 6.1-5, and the corresponding amplitude phase constellation is shown in Figure 6.1-6.

To demonstrate the effects of soft limiting, such as might occur in a Class C power amplifier, the modulators output waveform (previously shown in Figure 6.1-3, was mathematically soft limited. The resulting waveform is shown as Figure 6.1-7. An FFT of this waveform produces the spectrum shown in Figure 6.1-8. Note that the bandwidth efficiency remains 2 Bits/Hz, but a second harmonic component is generated. This

harmonic signal can be easily removed without in-band amplitude or phase distortion. Following quadrature detection of this limited waveform, the simulated received baseband tri-level signal is shown as Figure 6.1-9. The corresponding amplitude phase constellation is shown in Figure 6.1-10. Note that the expected square pattern has been compressed into a circular pattern by the soft limiting. This will introduce higher bit error rates as demonstrated in the next section.

The MATHCAD model was also used to demonstrate carrier reconstruction for the demodulator. After introducing channel noise to the soft-limited signal, the simulated received amplitude phase constellation becomes that shown in Figure 6.1-11. To implement the remod/demod carrier recovery, the reconstructed baseband signals remodulate the received carrier. The I channel signal is then shifted 90^{0} and added to the Q channel, resulting in the waveform shown in Figure 6.1-12. Note that the reconstructed carrier signal is null when either the I or Q baseband signal is zero. This will not cause a phase locking problem for the local oscillator since the error signal will be in a sample data loop.

As described above,this method of carrier reconstruction and local oscillator phase locking has already been demonstrated in the breadboard QPRS modem.

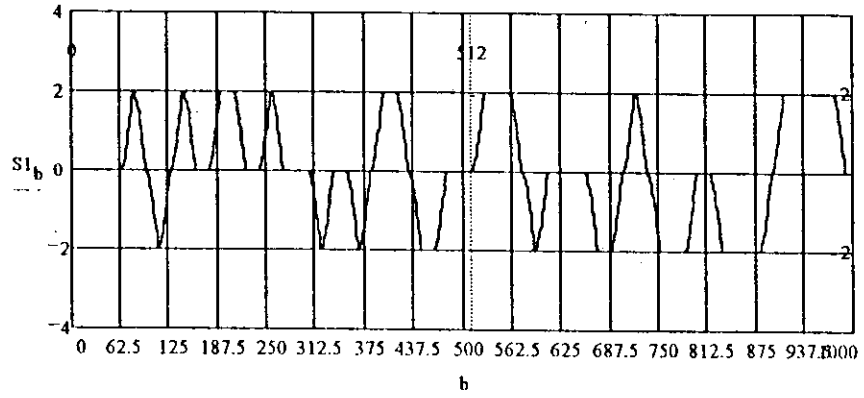

Figure 6.1-1) Simulated Modulator (D+1) Waveform

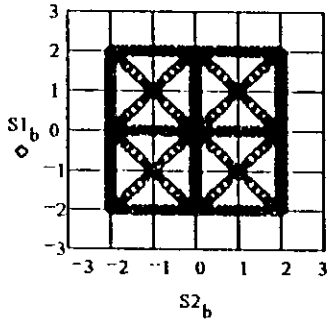

Figure 6.1-2) Simulated Modulator Amplitude Phase Constellation

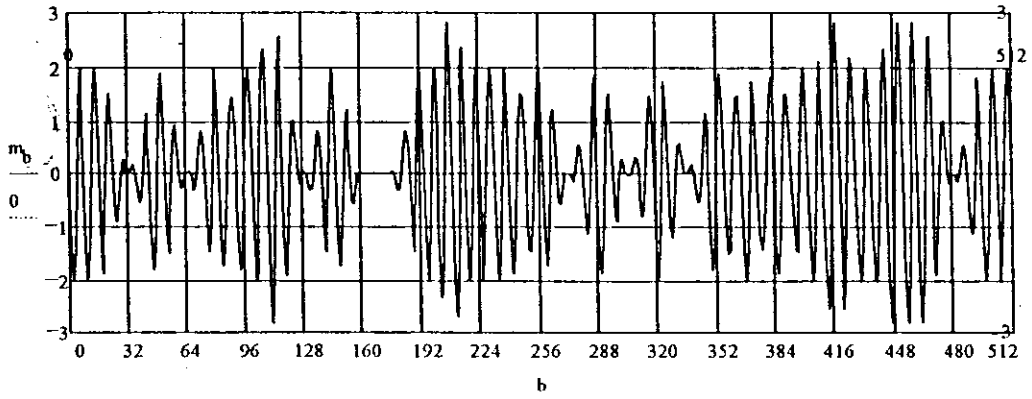

Figure 6.1-3) Simulated QPR Modulated Waveform

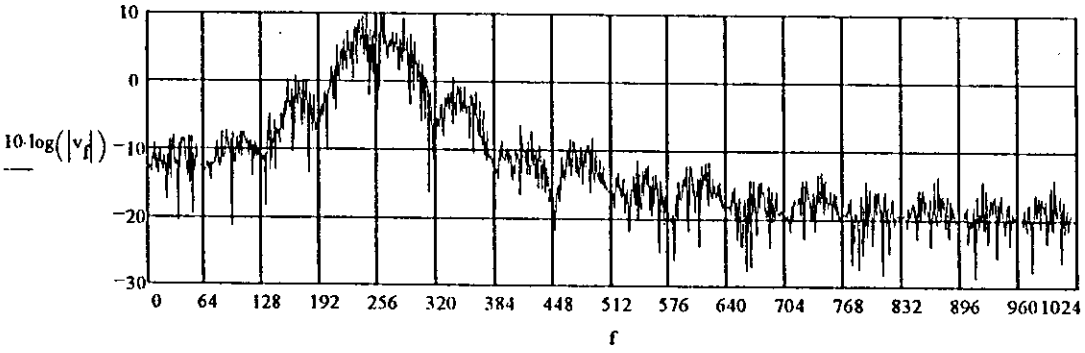

Figure 6.1-4) FFT of the QPR Modulated Waveform Demonstrating 2 Bits/Hz Bandwidth Efficiency

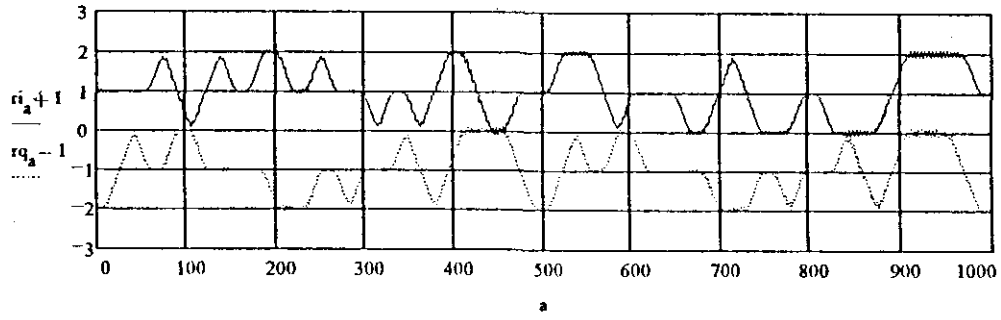

Figure 6.1-5) Simulated Received Baseband Waveform

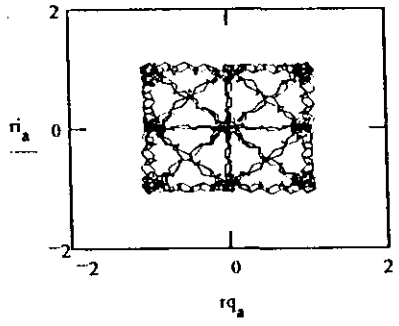

Figure 6.1-6) Simulated Received Amplitude Phase Constellation

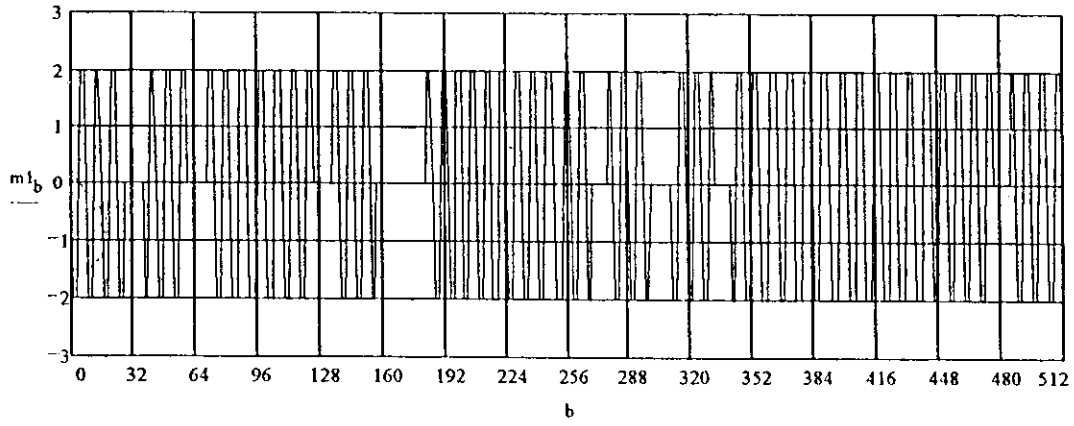

Figure 6.1-7) Simulated QPR Modulated Waveform with Soft Limiting

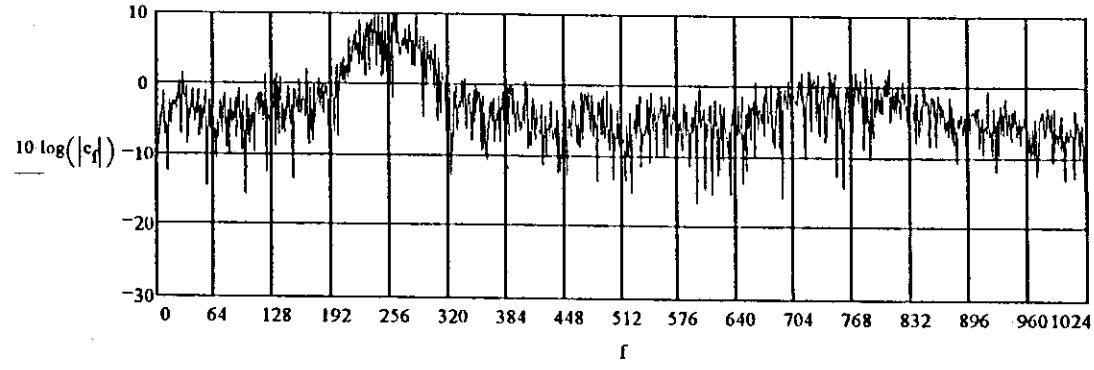

Figure 6.1-8) FFT of the Soft Limited QPR Modulated Waveform

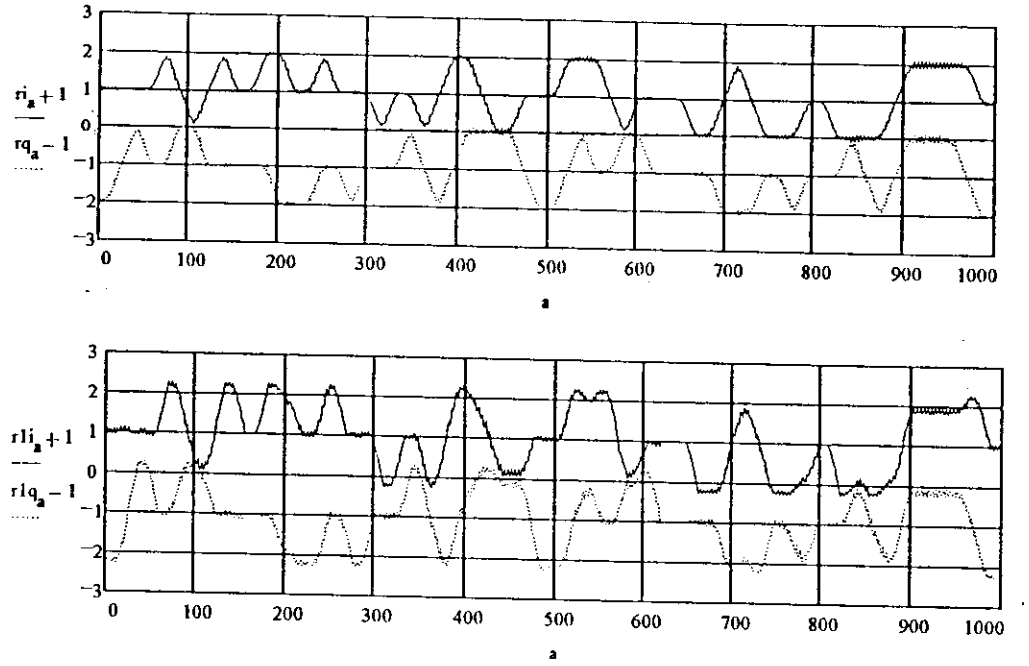

Figure 6.1-9) Simulated Received Baseband Waveform
with Soft Limiting at the Modulator

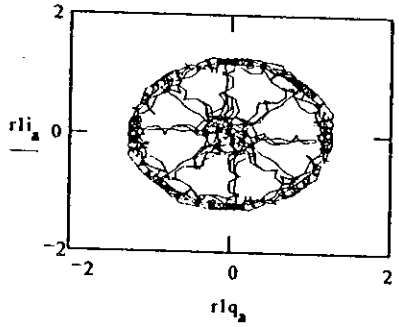

Figure 6.1-10) Simulated Received Amplitude Phase Constellation
with Soft Limiting at the Modulator

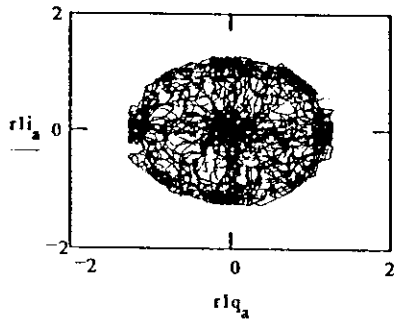

Figure 6.1-11) Simulated Received Amplitude Phase Constellation with Soft Limiting at the Modulator and AGWN Channel Noise

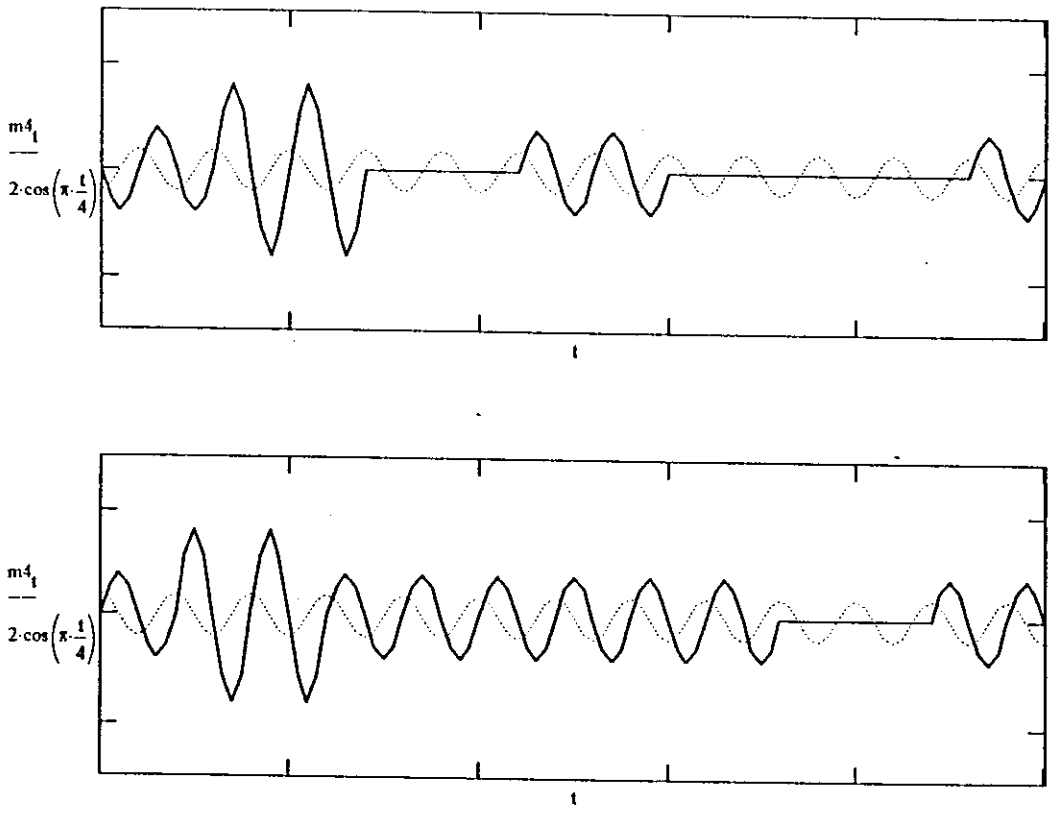

Figure 6.1-12) Reconstructed Carrier Signal for LO Phase Locking

6.2) Modem Simulation in the Presence of Noise

MMInc.'s custom QPRS modem simulator was used to simulate the performance of the high data rate modem with and without additive gaussian white noise in the channel. Simulated performance through various portions of the modulator and demodulator are shown in this section for comparison with the measured breadboard results the MATHCAD calculations. Bit error rate (BER) runs of the modem simulator in the presence of noise are presented at the end of this section. These bit error rate simulations entailed very long computer run times, clearly indicating the need for a breadboard modem. All of these simulations incorporated the newly designed data decoder.

Waveforms have been plotted for various locations within the simulated modulator and demodulator for comparison to measured wave shapes. Starting with the modulator, Figure 6.2-1 shows the I channel (D+1) tri-level signal generated by the QPRS algorithm following differential encoding of the digital input stream. The eye diagram of this waveform is shown in Figure 6.2-2, and the I/Q amplitude phase plot of the transmitter is shown in Figure 6.2-3. Following modulation, a discrete Fourier transform of the IF waveform produces the simulated spectrum shown in Figure 6.2-4. As measured with the aid of the breadboard modem, this spectrum clearly shows the QPRS modem's bandwidth efficiency of 2 Bits/Hz.

After detection in the demodulators I/Q mixers, and low pass filtering to remove mixer harmonic products and noise introduced in the channel, the received tri-level baseband I waveform (without additive noise in the channel model) is shown in Figure 6.2-5. Introduction of additive gaussian white noise results in the simulated received I waveform shown in Figure 6.2-6. The corresponding eye diagram of this waveform is shown in Figure 6.2-7 (without channel noise), and Figure 6.2-8 (with noise). The I/Q amplitude phase plot is shown in Figure 6.2-9 (without noise) and Figure 6.2-10 (with noise). Data decoding of these received waveforms is correct, as shown by the bit error rate "measurements" run on this simulator.

The simulated bit error rate performance of the high data rate, bandwidth efficient QPRS modem in the presence of additive gaussian white noise (AGWN) is summarized in Figure 6.2-11. In this figure, simulated performance at one dB intervals is superimposed on the theoretical curves previously shown as Figure2.0-1. Note that the simulated data points are virtually on top of the theoretical curve for QPRS modulation.

Due to the long computer run times involved, a complete curve for the many possible hardware imperfections such as phase imbalance, amplitude imbalance, threshold variations, and DC offset were not generated. Individual points were, however generated to investigate modem sensitivity to some of these imperfections. As an example of one of the more extensive of these calculations, Figure 6.2-12 shows the effect of a 10^{0} phase imbalance in the demodulators I/Q mixers.

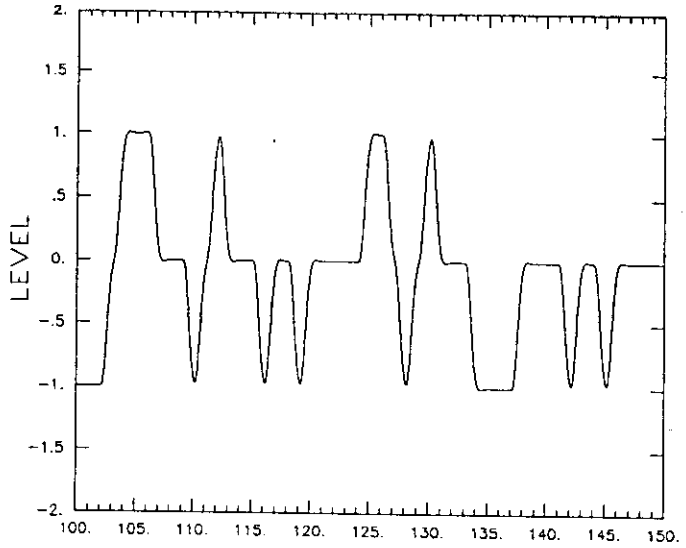

Figure 6.2-1) Simulated Modulator (D+1) Signal Waveform

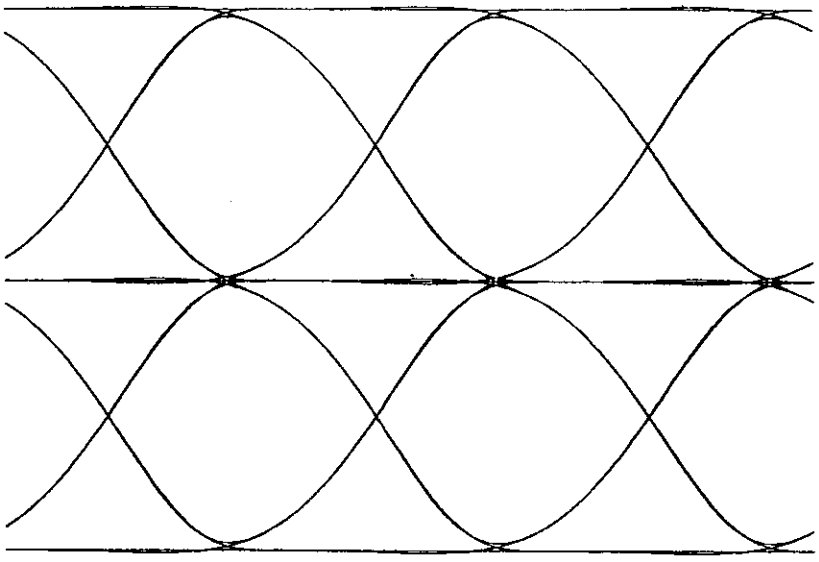

Figure 6.2-2) Simulated QPRS Modulator Eye Diagram

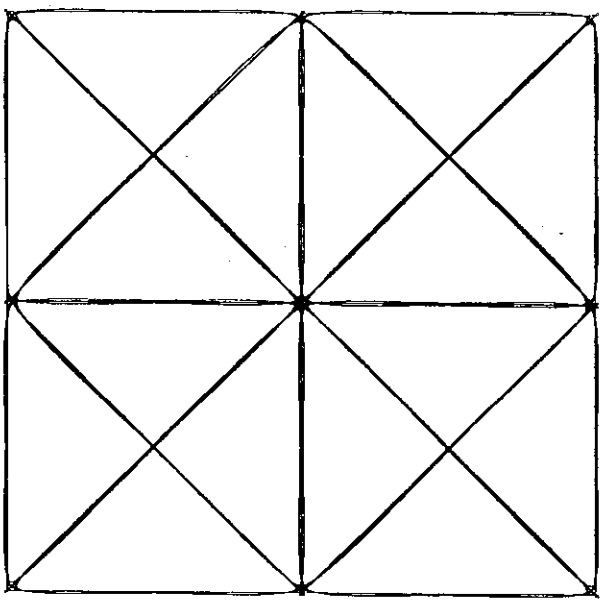

Figure 6.2-3) Simulated QPRS Modulator Amplitude Phase Plot

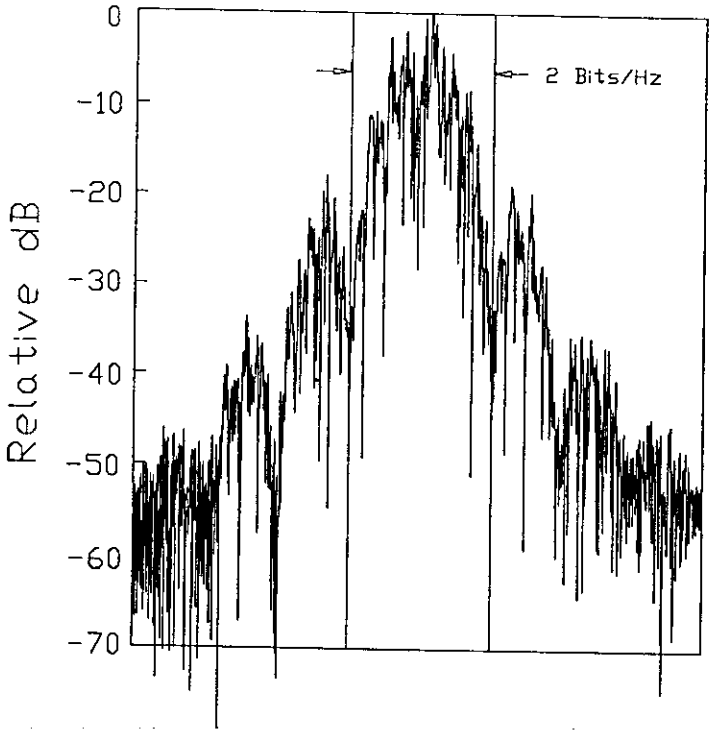

Figure 6.2-4) Unfiltered Spectrum of the Simulated QPRS Modulator Output Waveform, Showing 2 Bits/Hz Spectral Efficiency

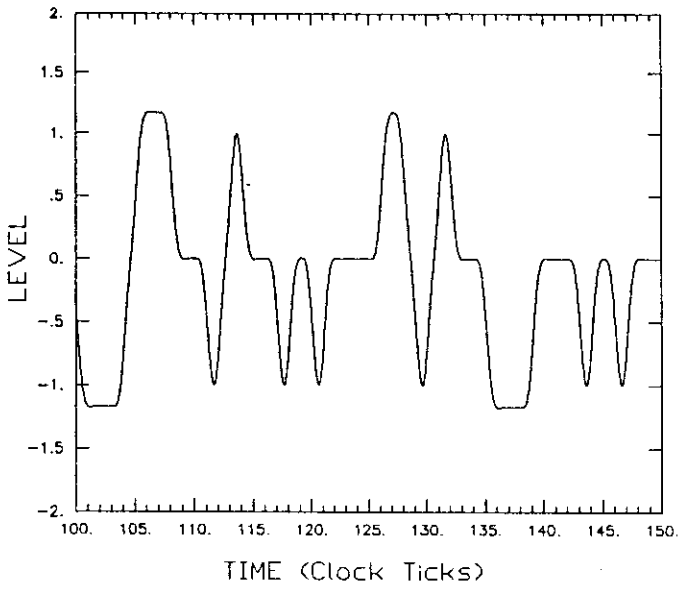

Figure 6.2-5) Simulated Tri-Level Received I Channel Waveform Without Channel Noise

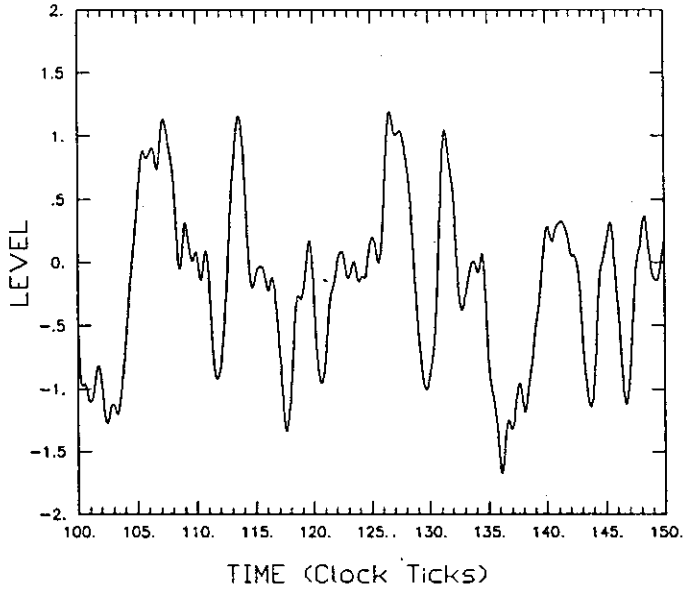

Figure 6.2-6) Simulated Tri-Level Received I Channel Waveform With Channel Noise

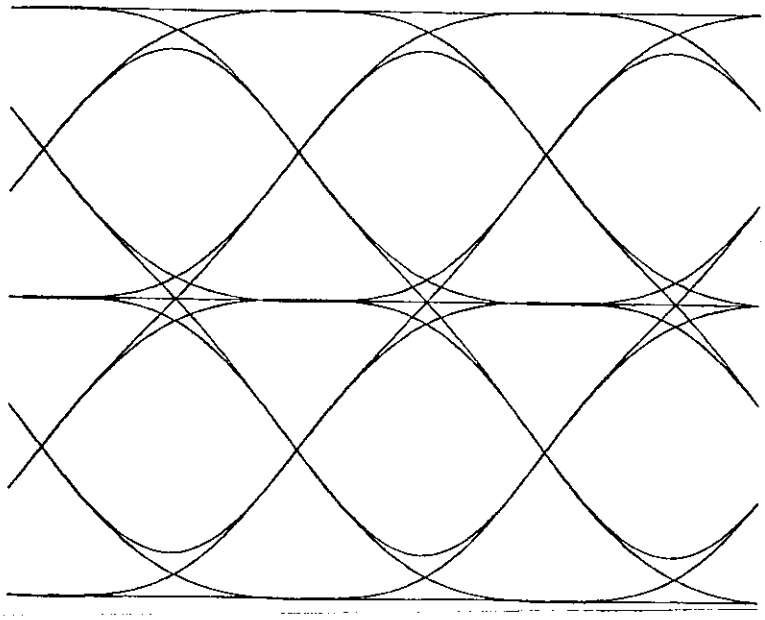

Figure 6.2-7) Eye Diagram of the Simulated Receiver I Channel Without Channel Noise

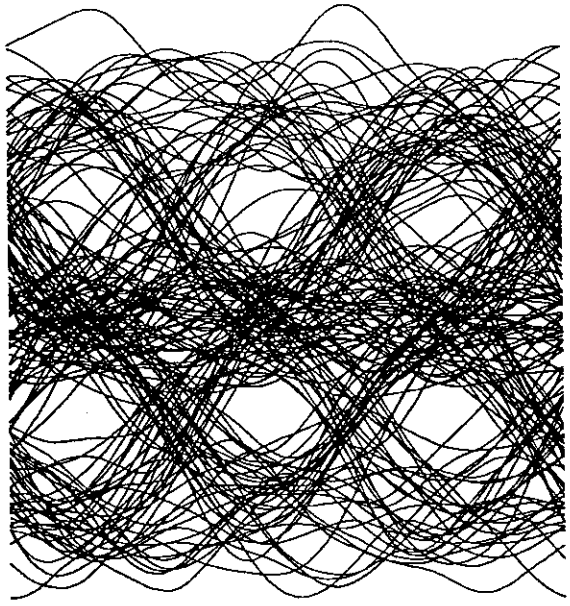

Figure 6.2-8) Eye Diagram of the Simulated Receiver I Channel With Channel Noise

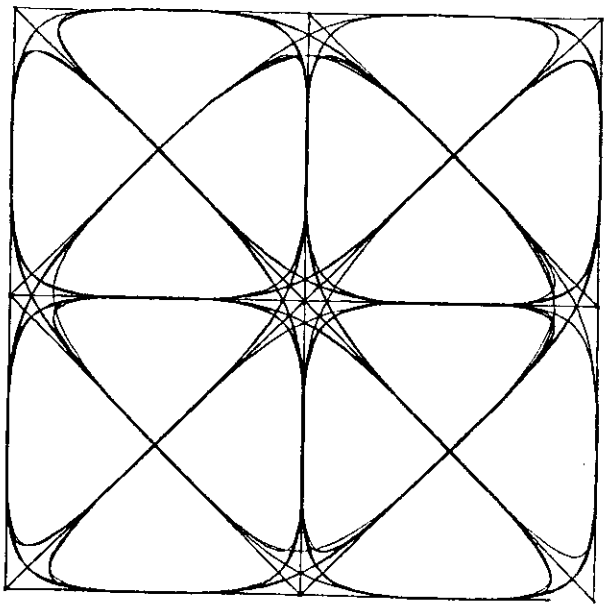

Figure 6.2-9) Simulated QPRS Demodulator Amplitude Phase Plot Without Channel Noise

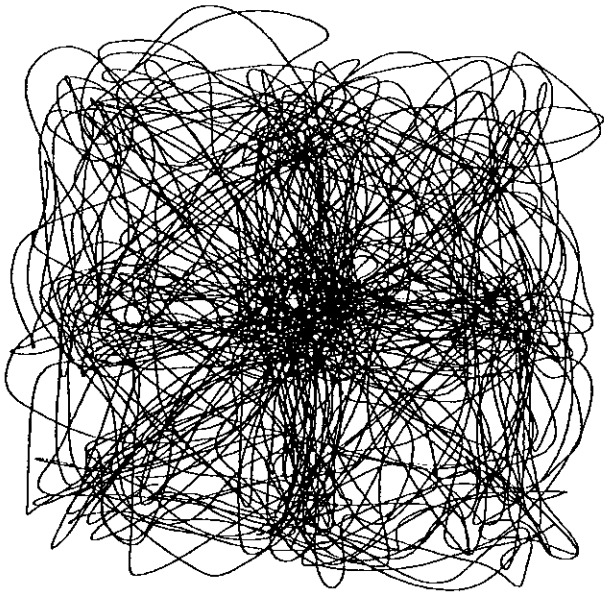

Figure 6.2-10) Simulated QPRS Demodulator Amplitude Phase Plot With Channel Noise

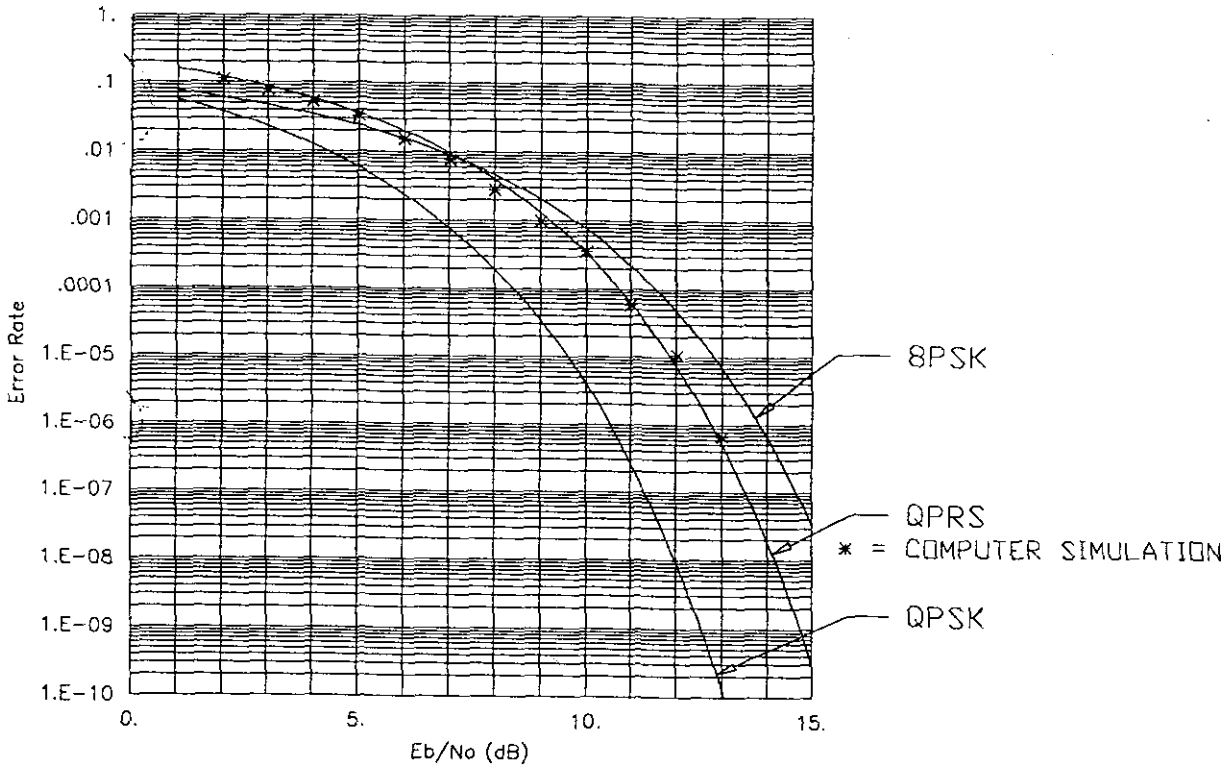

Figure 6.2-11) Simulated QPRS High Data Rate, Bandwidth Efficient Modem Bit Error Rate Performance Compared to Theory

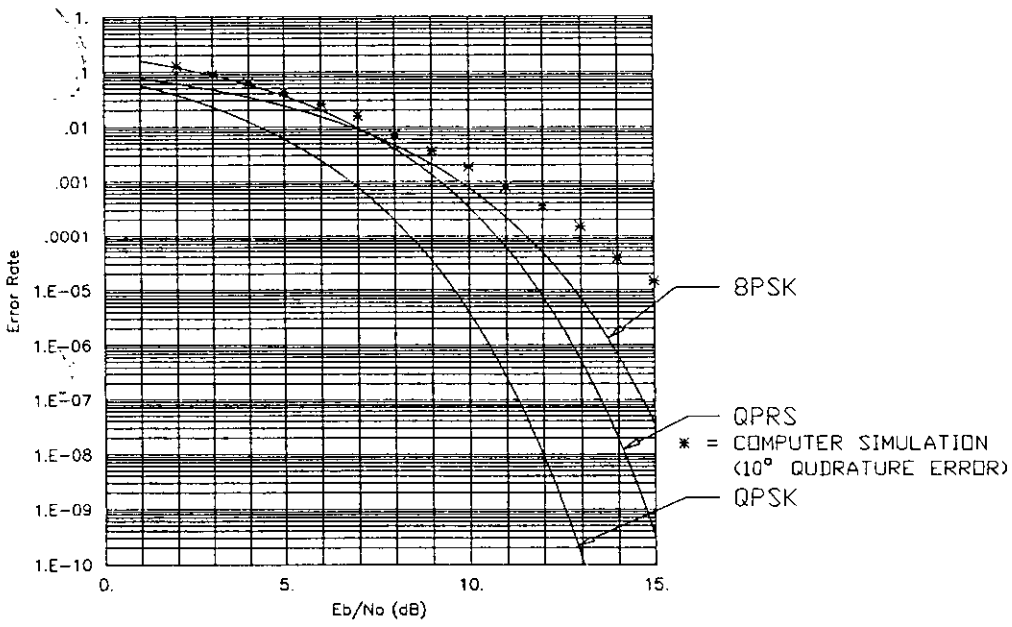

Figure 6.2-12) Simulated QPRS High Data Rate, Bandwidth Efficient Modem Bit Error Rate Performance with Phase Imbalance in the Demodulator I/Q Mixers

6.3) Modem Simulation in the Presence of Noise and Limiting

The internally developed modem simulator was also run with a simplified model of a limiting channel. To control computer run times, this analysis was performed at selected Eb/No ratios.

With the limiter driven into approximately 3 dB compression, the simulated performance in the presence of AGWN noise degraded by only 2 dB at an error rate of 10^{-4}, and 2.5 dB at an error rate of 10^{-6}. Note that this analysis is very preliminary since a simplified limiter which does not include AM to PM conversion effects was implemented, and the demodulator filters were sub-optimum.

A single simulation run was also made with the limiter driven into 1 dB compression. This run produced a degradation of about 1 dB at an error rate of 10^{-4}.

7) Enhanced Bandwidth Efficient Breadboard Modem

As the program progressed, the necessity of a low frequency, low data rate, bandwidth efficient breadboard modem such as MMInc.'s existing breadboard became increasingly clear. Although this existing breadboard provided many valuable insights and extensive data, including all of the measured data presented in this report, it became obvious that a second generation breadboard would be needed during phase II. Although not originally proposed as part of the phase I effort, MMInc. therefore decided to construct a second generation low data rate, bandwidth efficient modem which is more versatile than the original. Fabrication could not be completed within the constraints of program phase I, however construction is well under way, thus providing a "head start" on the proposed phase II effort. The new breadboard contains the design changes developed under phase I, and operates at a somewhat higher carrier frequency (70 MHz) and data rate (2 Mbps) to further ease experimentation.

A photograph of the completed portion of this second generation breadboard modem is shown in Figure 7-1.

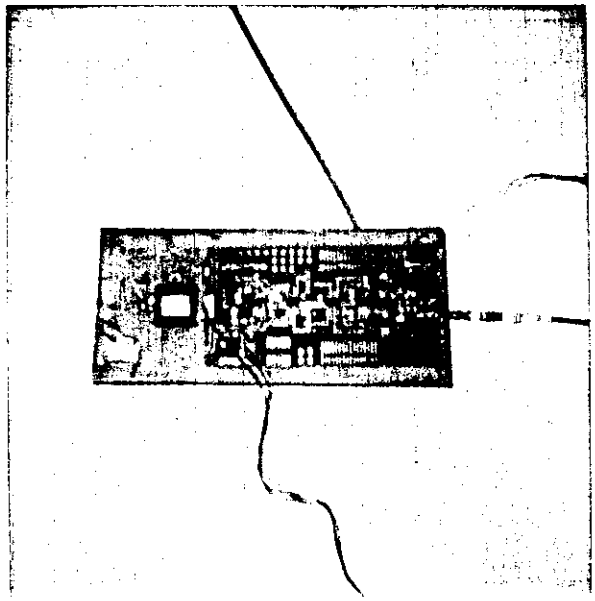

Figure 7-1) Photograph of a portion of the second generation Breadboard Modem, providing a "head start" on Phase II.

8) High Data Rate Modem Design Modifications

As previously described, both experimental measurements and computer analysis clearly indicate that the preliminary high data rate modem design originally submitted with the phase I proposal is a solid design. Detailed evaluation of the modem performance characteristics in the presence of noise have, however, indicated that a more robust data detector is required.

Specifically, certain transitions in the received I and Q signal channels are invalid. For example, a direct transition from positive to negative without an interim zero voltage signal is invalid since such a transition can not be generated by the modulator. This and related transition constraints are, in fact, what give the QPRS modulator its superior bandwidth efficiency properties. The same constraints can, and should, be used to perform "error correction" in the data detector.

Such "error correction" is not the same as traditional techniques which introduce overhead bits into the input data stream. In the case of QPR signaling the correction information is inherent in the transmitted waveform, and no additional overhead, which would effectively reduce the bandwidth efficiency, is required. A circuit which implements this no-overhead enhanced data detection is shown in Figure 8-1.

It must be noted that implementation of this enhanced data detector does not preclude the simultaneous use of standard error correction techniques. In fact the QPRS modem is particularly well suited to take advantage of these techniques if desired.

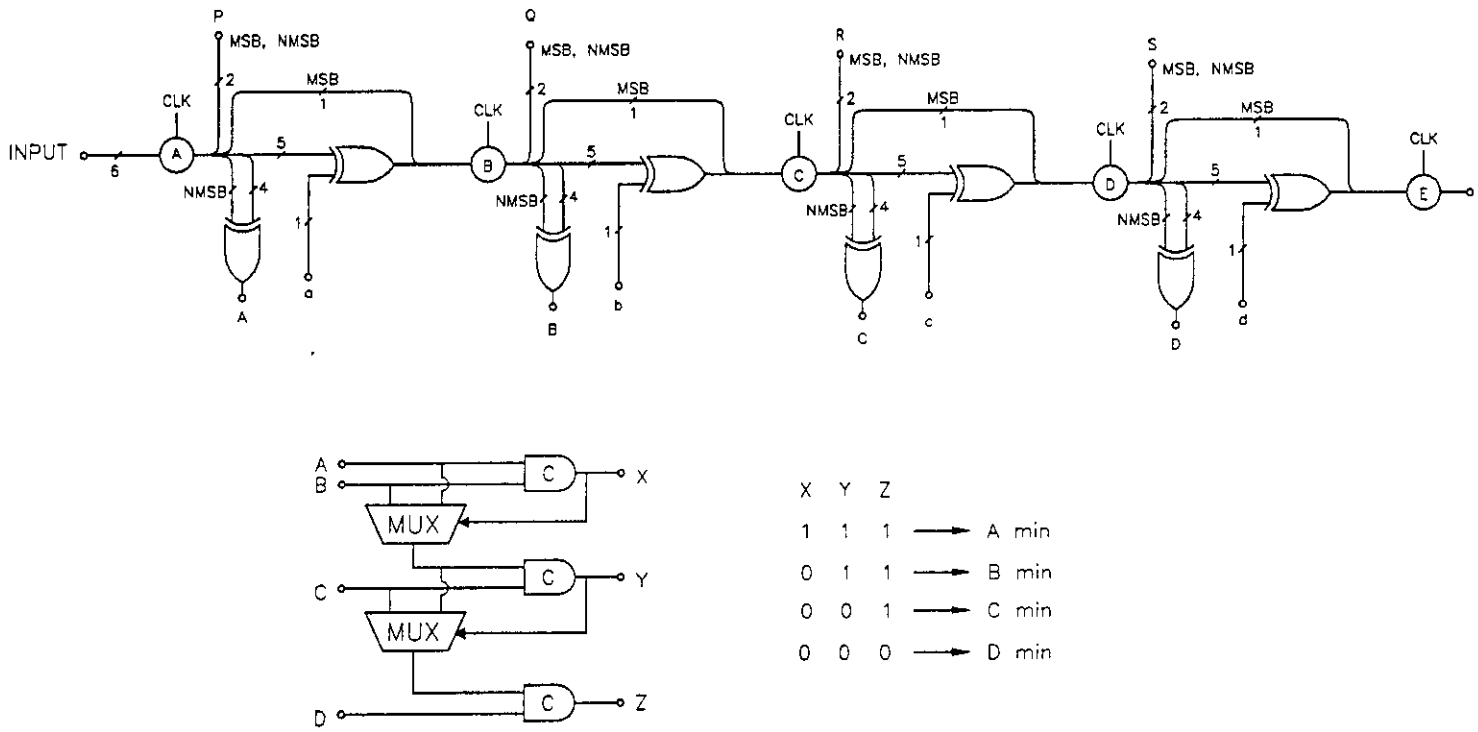

Figure 8-1) Preliminary Design of the Enhanced Data Detector Circuit

9) CONCLUSIONS

Despite a severe interruption caused by the "Northridge" earthquake on January 17, 1994, all of the Phase I tasks have been completed on time. The exciting results from this program clearly indicate that a rugged, low power, bandwidth efficient, high data rate modem based on MMInc.'s approach is ideally suited to advanced satellite communications systems, where bandwidth and prime power are at a premium. A phase II proposal has therefore been submitted to fabricate an engineering prototype of the high data rate bandwidth efficient modem designed in phase I, and deliver it to NASA.

Key performance goals for the bandwidth efficient, high data rate modem include a spectral efficiency of 2 Bits/Hz at a data rate of 800 Mbps, an implementation loss less than 3 dB from QPSK at a BER of 10^{-6} with AGWN, and an IF center frequency of 3.239 GHz. These goals, particularly bandwidth, IF frequency, and data rates, have been selected for maximum compatibility with on-going NASA programs, as well as to demonstrate the capabilities of the modem.

The experimental, theoretical, and computer aided design results of phase I have clearly demonstrated feasibility of MMInc.'s modem design, thus providing a strong foundation for the phase II program.

10) REFERENCES

[1] A Lender, The Duobinary Technique For High Speed Data Transmission, IEEE Trans. Comm and Elec. Vol. 82 pp 214-218 May 1963.

[2] Taylor and Cheung, Decision Directed Carrier Recovery Loop for QPRS, IEEE Com. Vol 27 February 1979.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

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1. AGENCY USE ONLY (*Leave blank*)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	June 1994	Final Contractor Report

4. TITLE AND SUBTITLE

Power and Spectral Efficient Advanced High Data Rate Modem

5. FUNDING NUMBERS

WU–324–01–00
NAS3–26965

6. AUTHOR(S)

Wendell C. Peterson and Daniel Ch'en

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

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8. PERFORMING ORGANIZATION REPORT NUMBER

E–8887

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

National Aeronautics and Space Administration
Washington, D.C. 20546–0001

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

NASA CR–195338

11. SUPPLEMENTARY NOTES

Project Manager, William D. Ivancic, Communications Technology Division, NASA Glenn Research Center, organization code RCN, 216–433–3494.

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13. ABSTRACT ***(Maximum 200 words)***

The exponentially increasing demand to transfer massive amounts of data between world wide destinations generated by sophisticated space and ground based high resolution multi-band sensors, interactive multi-media, computer network interlinks, and wireless trunkline systems is severely straining the available microwave bandwidth, which can only grow linearly by costly extension into the millimeter-wave bands. Power and spectrally efficient, high data rate modems are thus essential, particularly at high concentration "bottle necks" which typically occur in the space segment of communications backbones such as those planned for deployment over the next decade. Microwave Monolithics Incorporated (MMInc.) has identified a superior approach to meet this need, and has clearly demonstrated feasibility of its approach in this Phase I program via extensive computer simulations and experimental characterization of a bandwidth efficient, lower data rate breadboard modem. MMInc.'s high data rate (800 Mbps), spectrally efficient (2 Bits/Hz) modem design has been "tweaked" and is now ready for implementation and in Phase II, which would culminate in the delivery of an engineering prototype modem to NASA followed by commercialization in Phase III.

14. SUBJECT TERMS	15. NUMBER OF PAGES
PCM modulation; Satellite communications; Integrated circuits	58
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	